

CLAIMS

What is claimed is:

1. A signal pathway configured to minimize signal reflections and signal degradation, comprising:
 - 5 a first signal line formed on and extending across a circuit board, the first signal line having a first end configured for electrical coupling with a clock driver chip and a second end forming a first terminal;
 - a second signal line formed on a circuit component and electrically coupled with the first terminal of the first signal line at a first pad, the second
 - 10 signal line extending from the first pad and having a portion forming a stub within the circuit component;
 - a third signal line electrically coupled with the second signal line and extending therefrom at a point within the circuit component to a second pad; and
 - 15 a fourth signal line formed on and extending across the circuit board, the fourth signal line having a first end electrically coupled with the third signal line at the second pad and forming a second terminal, and a second end forming a termination;
 - whereby clock signals may be carried by the first, second, third and fourth
 - 20 signal lines from the clock driver chip to the stub and on to the termination.
2. The signal pathway of claim 1, wherein the circuit component comprises an integrated circuit with a package and a die mounted within the package, the stub having a terminating end extending into the integrated circuit.
- 25 3. The signal pathway of claim 2, wherein the point within the circuit component from which the third signal pathway extends is in a region within the package.

4. The signal pathway of claim 1, wherein the circuit component comprises a package and a die mounted within the package, the stub having a terminating end extending to the die.
5. The signal pathway of claim 4, wherein the point within the circuit component from which the third signal pathway extends is in a region within the package.
6. The signal pathway of claim 1, wherein the stub has a length of about 2 mm or less.
7. The signal pathway of claim 1, wherein the first pad and the second pad are each ball grid array pads.
8. The signal pathway of claim 1, wherein the termination comprises at least one termination resistor.
9. The signal pathway of claim 8, wherein the impedance of the termination resistor is approximately the same as the total impedance of the signal pathway up to the termination resistor.
10. A signal pathway formed on an circuit component, the circuit unit comprising a package and a die to form an integrated circuit chip mounted on a surface, the signal pathway comprising:
- a first signal line portion extending into the package from a signal-in pad disposed on a surface thereof opposite of the integrated circuit chip, the first signal line portion forming a stub extending at least to an interface of the integrated circuit chip die and the package to be in electrical connection with the circuit chip; and
- a second signal line portion branching from the first signal line portion at a base of the stub and extending to a signal-out pad disposed on the surface of the package adjacent to the signal-in pad;
- whereby clock signals may enter the intergrated circuit unit at the signal-in pad and exit the unit at the signal-out pad.

11. The signal pathway of claim 10, wherein the stub has a length of about 2 mm or less.

12. The signal pathway of claim 10, wherein the stub extends into the integrated circuit chip.

13. A signal pathway for carrying clock signals from a clock driver to a circuit component mounted to a circuit board, the signal pathway having a termination on the circuit board and configured to minimize signal reflections and signal degradation, the signal pathway comprising:

10 a first signal line formed on a circuit board and electrically connected to a clock driver, the first signal line extending to a first terminal;
a second signal line formed on the circuit board and extending from a second terminal to a termination;
a third signal line formed in the circuit component, the third signal line
15 extending from a Signal In pad electrically coupled with the first terminal to a Signal Out pad electrically coupled with the second terminal; and
a stub electrically coupled with the second signal line on the circuit component.

14. The signal pathway of claim 13, wherein the circuit component comprises a package and a die within the package, the stub extending to the die for electrical connection therewith.

15. The signal pathway of claim 13, wherein the stub has a length of about 2 mm or less.

16. The signal pathway of claim 13, wherein the termination comprises at least one termination resistor.

17. The signal pathway of claim 16, wherein the impedance of the termination resistor is approximately the same as the total impedance of the signal pathway up to the termination resistor.

18. An electronic system, comprising:

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a circuit board having an interface;

a circuit component mounted onto the circuit board interface to electrically couple the circuit component to the circuit board; and

a signal pathway, comprising:

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a first signal line formed on the circuit board and electrically connected to a clock driving means, the first signal line extending to a first terminal;

a second signal line formed on the circuit board and extending from a second terminal to a termination;

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a third signal line formed on the circuit component, the second signal line extending from a Signal In pad electrically coupled with the first terminal at the circuit board interface to a Signal Out pad electrically coupled with the second terminal at the interface; and

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a stub electrically coupled with the second signal line on the circuit component.

wherein the clock driving means generates clock signals to be carried by the signal pathway to the circuit component and on to the termination.

19. The system of claim 18, wherein the circuit component comprises a package and a processing chip mounted with the package, the stub extending to the chip for electrical connection therewith.

20. The system of claim 18, wherein the circuit component comprises an integrated circuit made up of a package and a die mounted within the package, the stub extending to the chip for electrical connection therewith.

21. The system of claim 18, wherein the stub has a length of about 2 mm or less.

22. A method for routing a clock signal to a receiver whereby a waveform of the clock signal has an acceptably low amount of noise at the receiver, the receiver comprising an circuit component, the method comprising the steps of:

providing a signal pathway, comprising:

- 5 a first signal line formed on a circuit board and electrically connected to a clock driver, the first signal line extending to a first terminal;
 - a second signal line formed on the circuit board and extending from a second terminal to a termination;
 - 10 a third signal line formed on the circuit component mounted with the circuit board, the second signal line extending from a Signal In pad electrically coupled with the first terminal to a Signal Out pad electrically coupled with the second terminal; and
 - 15 a stub electrically coupled with the second signal line on the circuit component; and
- driving the clock signal, by the clock driver, along the signal pathway to the circuit component and on to a termination.

23. The method of claim 22, wherein the circuit component comprises a package and a processing chip mounted with the package, the stub having a
- 20 terminating end disposed with the chip, and wherein the step of driving a clock signal comprises driving the clock signal, by the clock driver, along the signal pathway to the processing chip and on to the termination.

24. The method of claim 22, wherein the circuit component comprises a package and a die mounted with the package, the stub having a terminating end
- 25 disposed with the chip, and wherein the step of driving a clock signal comprises driving the clock signal, by the clock driver, along the signal pathway to the combined memory and I/O controller chip and on to the termination.

25. The method of claim 22, whereby when the clock signal waveform has a cycle time of at least about 300 MHz, the clock signal voltage measured at the

circuit component does not exceed about 1.2 volts and does not drop below about - 0.25 volts.